GENERAL DESCRIPTION

The W74LVC2G74 is a single positive-edge triggered D-type flip-flop with individual data (D) inputs, clock ($\overline{CP}$) inputs, set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

FEATURES

- Wide supply voltage range from 1.65V to 5.5V
- 5 V tolerant outputs for interfacing with 5 V logic
- ±24mA output drive (VCC=3.0V)
- CMOS low power consumption
- Latch-up performance exceeds 250mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5V
- Specified from -40℃ to +85℃
- Packaging information information: TSSOP8 /VSSOP8

BLOCK DIAGRAM

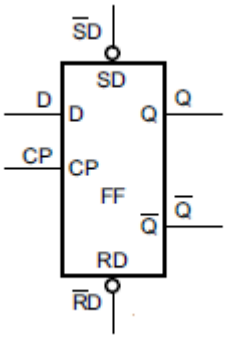


Figure 1. Logic symbol

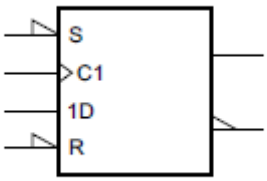


Figure 2. IEC logic symbol

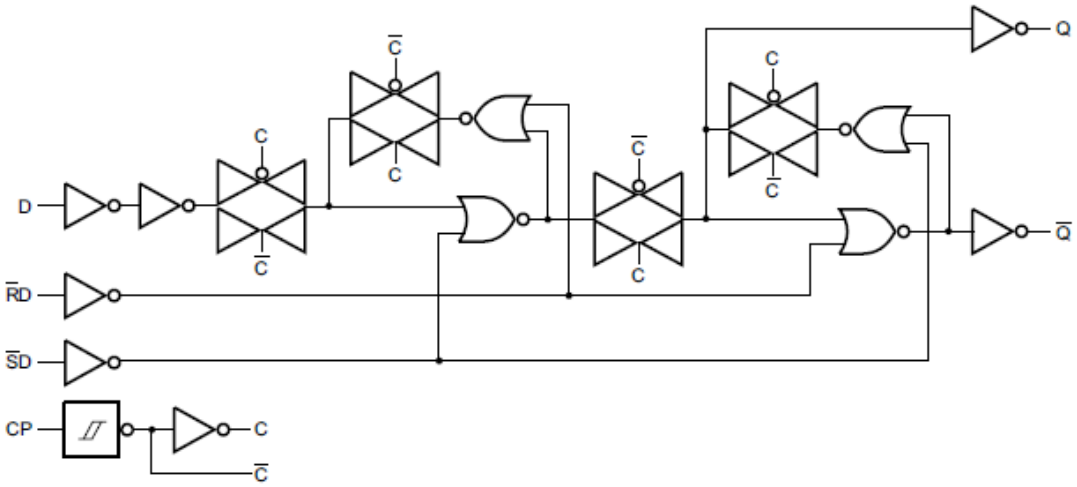
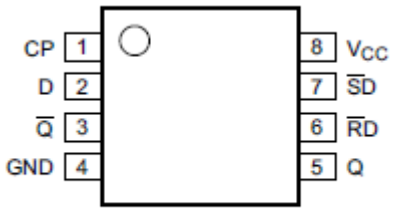


Figure 3. Logic diagram

PIN CONFIGURATION

Marking : AR



Pin Description

Pin No.	Pin Name	Description
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	D	data input
3	$\overline{Q}$	complement output
4	GND	ground (0V)
5	Q	true output
6	$\overline{RD}$	asynchronous reset-direct input (active LOW)
7	$\overline{SD}$	asynchronous set-direct input (active LOW)
8	V_{CC}	supply voltage

Function Table

Function table for asynchronous

operation	Input			Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

Function table for synchronous operation

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH CP transition;
Q_{n+1}=state after the next LOW-to-HIGH CP transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I < 0V	-50	-	mA
input voltage	V_I	-	-0.5	+6.5	V
output clamping current	I_{OK}	V_O > V_{CC} or V_O < 0V	-	±50	mA
output voltage	V_O	Active mode	-0.5	V_{CC}+0.5	V
		Power-down mode; V_{CC}=0V	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
total power dissipation	P_{tot}	-	-	300	mW
storage temperature	T_{stg}	-	-65	+150	℃
Soldering temperature	T_L	10s	250		℃

Note:

[1] For TSSOP8 package: above 55℃ the value of P_{tot} derates linearly with 2.5mW/K.

[2] For VSSOP8 package: above 110℃ the value of P_{tot} derates linearly at 8mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC}=0V	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+85	℃
input transition rise and fall rate	Δt/ΔV	V_{CC}=1.65V to 2.7V	-	-	20	ns/V
		V_{CC}=2.7V to 5.5V	-	-	10	ns/V

Electrical Characteristics

DC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V		0.65× V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7× V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		-	-	0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3× V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 5.5V	V_{CC}-0.1	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	1.54	-	V
			I_O=-8mA; V_{CC}=2.3V	1.9	2.15	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	2.50	-	V
			I_O=-24mA; V_{CC}=3.0V	2.3	2.62	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	4.11	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 5.5V	-	-	0.10	V
			I_O=4mA; V_{CC}=1.65V	-	0.07	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	0.12	0.30	V
			I_O=12mA; V_{CC}=2.7V	-	0.17	0.40	V
			I_O=24mA; V_{CC}=3.0V	-	0.33	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	0.39	0.55	V
input leakage current	I_I	V_I=5.5V or GND; V_{CC}=0V to 5.5V		-	±0.1	±1	uA
power-off leakage current	I_{OFF}	V_I or V_O=5.5V; V_{CC}=0V		-	±0.1	±2	uA
supply current	I_{CC}	V_I=5.5V or GND; I_O=0A; V_{CC}=1.65V to 5.5V		-	0.1	4	uA
additional supply current	ΔI_{CC}	per pin; V_I=V_{CC}-0.6V; I_O=0A; V_{CC}=2.3V to 5.5V		-	5	500	uA
input capacitance	C_I	-		-	4.0	-	pF

Note: All typical values are measured at T_{amb}=25℃.

AC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	CP to Q, $\overline{Q}$; see Figure 5	V_{CC}=1.65V to 1.95V	1.5	6.0	13.4	ns
			V_{CC}=2.3V to 2.7V	1.0	3.5	7.1	ns
			V_{CC}=2.7V	1.0	3.5	7.1	ns
			V_{CC}=3.0V to 3.6V	1.0	3.5	5.9	ns
			V_{CC}=4.5V to 5.5V	1.0	2.5	4.1	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	1.5	6.0	12.9	ns
			V_{CC}=2.3V to 2.7V	1.0	3.5	7.0	ns
			V_{CC}=2.7V	1.0	3.5	7.0	ns
			V_{CC}=3.0V to 3.6V	1.0	3.0	5.9	ns
			V_{CC}=4.5V to 5.5V	1.0	2.5	4.1	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 6	V_{CC}=1.65V to 1.95V	1.5	5.0	12.9	ns
			V_{CC}=2.3V to 2.7V	1.0	3.5	7.0	ns
			V_{CC}=2.7V	1.0	3.5	7.0	ns
			V_{CC}=3.0V to 3.6V	1.0	3.0	5.9	ns
			V_{CC}=4.5V to 5.5V	1.0	2.5	4.1	ns
pulse width	t_W	CP HIGH or LOW; see Figure 5	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	1.3	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; see Figure 6	V_{CC}=1.65V to 1.95V	6.2	-	-	ns
			V_{CC}=2.3V to 2.7V	2.7	-	-	ns
			V_{CC}=2.7V	2.7	-	-	ns
			V_{CC}=3.0V to 3.6V	2.7	1.6	-	ns
			V_{CC}=4.5V to 5.5V	2.0	-	-	ns
recovery time	t_{rec}	$\overline{SD}$ or $\overline{RD}$; see Figure 6	V_{CC}=1.65V to 1.95V	1.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.4	-	-	ns
			V_{CC}=2.7V	1.3	-	-	ns
			V_{CC}=3.0V to 3.6V	+1.2	-3.0	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
set-up time	t_{su}	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	2.9	-	-	ns
			V_{CC}=2.3V to 2.7V	1.7	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.3	0.5	-	ns
			V_{CC}=4.5V to 5.5V	1.1	-	-	ns
hold time	t_h	D to CP; see Figure 5	V_{CC}=1.65V to 1.95V	1.5	-	-	ns
			V_{CC}=2.3V to 2.7V	1.0	-	-	ns
			V_{CC}=2.7V	1.0	-	-	ns
			V_{CC}=3.0V to 3.6V	1.0	0.6	-	ns
			V_{CC}=4.5V to 5.5V	1.0	-	-	ns
maximum frequency	f_{max}	CP; see Figure 5	V_{CC}=1.65V to 1.95V	80	-	-	MHz
			V_{CC}=2.3V to 2.7V	175	-	-	MHz

			V_{CC}=2.7V	175	-	-	MHz
			V_{CC}=3.0V to 3.6V	175	280	-	MHz
			V_{CC}=4.5V to 5.5V	200	-	-	MHz
Power dissipation capacitance	C_{PD}	V_{CC}=3.3V; V_I=GND to V_{CC}		-	15	-	pF

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}\times V_{CC}^2\times f_i\times N)+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

Testing Circuit

AC Testing Circuit

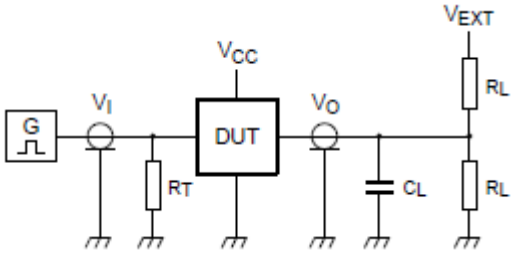


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance; should be equal to the output impedance Z_o of the pulse generator. V_{EXT}=External voltage for measuring switching times.

AC Testing Waveforms

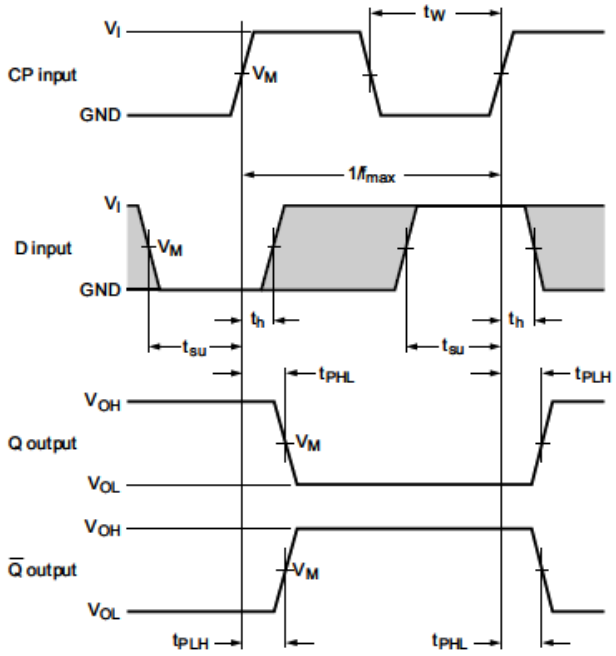


Figure 5. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum frequency

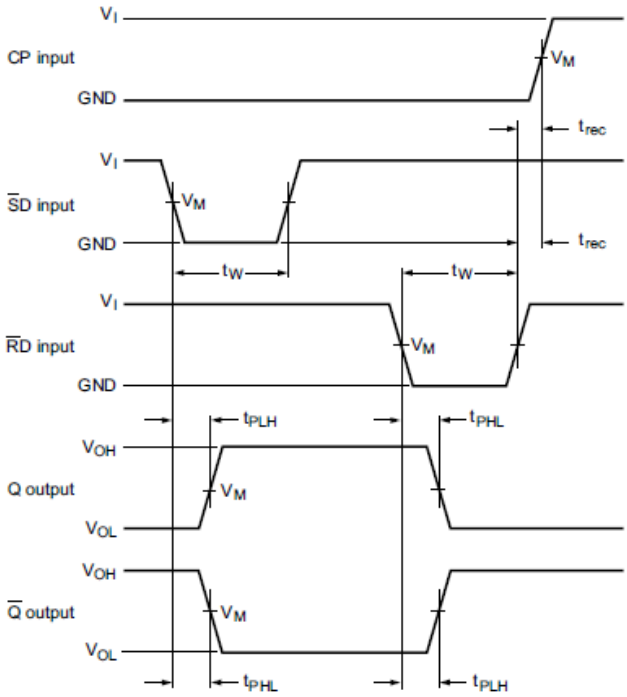


Figure 6. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{RD}$ to CP recovery time

Measurement Points

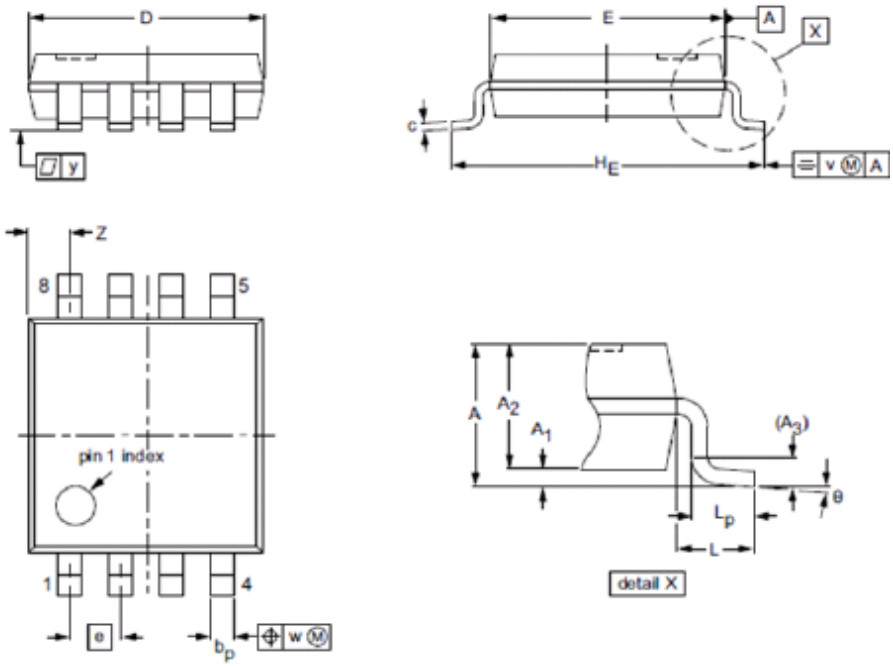
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Test Data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	open	GND	$2 \times V_{CC}$
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	open	GND	$2 \times V_{CC}$
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	open	GND	6V
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	open	GND	6V
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	open	GND	$2 \times V_{CC}$

Outline Drawing

TSSOP8

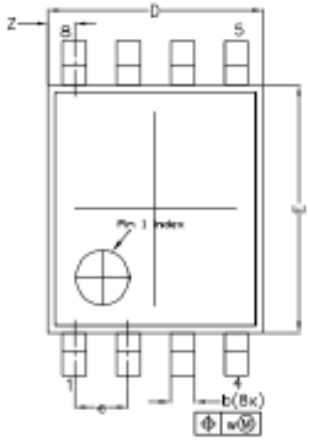


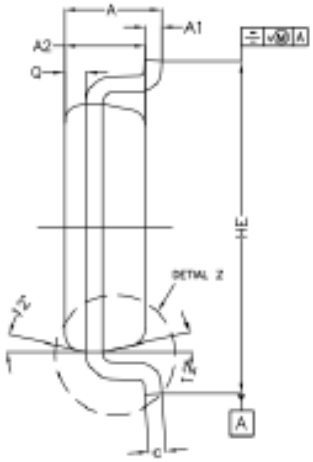
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.1		0.043
A1	0.000	0.150	0.000	0.006
A2	0.75	0.95	0.03	0.037
A3	0.25 Typ.		0.01 Typ.	
bp	0.22	0.38	0.009	0.015
c	0.08	0.18	0.003	0.007
E(1)	2.90	3.10	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
H_E	3.90	4.10	0.154	0.161
L	0.50		0.020	
Lp	0.33	0.47	0.013	0.019
v	0.20		0.008	
w	0.13		0.005	
y	0.10		0.004	
Z(1)	0.35	0.70	0.014	0.028
θ	0°	8°	0°	8°

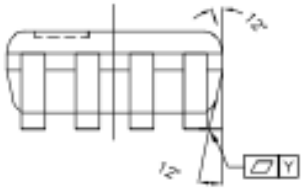
Rev.A

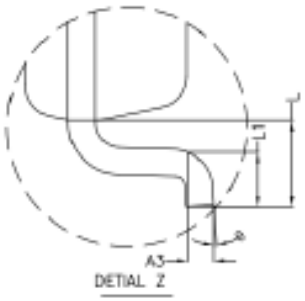
Outline Drawing

VSSOP8









* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.00	---	0.15
A2	0.60	0.75	0.85
A3	---	0.12	---
Q	0.19	0.20	0.21
b	0.17	0.22	0.27
c	0.08	---	0.23
D	1.90	2.00	2.10
E	2.20	2.30	2.40
HE	3.00	3.10	3.20
e	0.50 bsc		
L	0.40 bsc		
L1	0.15	---	0.40
Y	---	0.10	---
v	---	0.20	---
w	---	0.08	---
Z	0.10	---	0.40
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Rev.A

Ordering Information:

Device PN	Packing
W74LVC2G74O(4)-T(1)H(2)-WS(3)	Tape&Reel: 6 Kpcs/Reel
W74LVC2G74V(4)-T(1)H(2)-WS(3)	Tape&Reel: 3 Kpcs/Reel

Note: (1) Packing code, Tape & Reel Packing

(2) Halogen free product for packing code suffix "H"

(3) WS : Willas brand abbreviation, Label Type does not display

(4) O : TSSOP8,V : VSSOP8